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TECHNICAL NOTE

Patterned cracks improve yield in the release of compliant microdevices from silicon-on-insulator wafers

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Abstract
The safe release of compliant structures is an ongoing challenge in microfabrication. The buried oxide (BOX) layer of silicon-on-insulator wafers is useful as an etch stop or sacrificial layer. However, when freed during processing, the BOX layer can buckle and crack from compressive stress, and these cracks can threaten the survival of delicate devices above the BOX layer. This work reports on the use of cracks patterned lithographically into the BOX layer prior to device release in two separate microcantilever fabrication processes. In both processes, the patterned cracks were found to inhibit spontaneous cracking in critical regions near or under devices and improve device yield. In the first process, the average yield of ultrasoft silicon cantilevers for magnetic resonance force microscopy improved by more than 60%. In the second process, the yield of piezoresistive silicon cantilevers for high-frequency force detection improved by more than 95% with the use of patterned cracks.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The buried oxide (BOX) layer of silicon-on-insulator (SOI) wafers is frequently employed as an etch stop and sacrificial layer in microfabrication [1]. However, compressive stress in the BOX layer can cause it to buckle and crack when the underlying silicon handle wafer is removed [2]. Compliant structures in the silicon device layer are susceptible to damage and fracture from cracks that form in the BOX layer during release processing.

As thermally-grown silicon dioxide, the BOX layer is usually under substantial compressive stress (300–500 MPa), due to the mismatch between the thermal expansion coefficients of silicon and silicon dioxide [3, 4]. Intrinsic stress from the volumetric expansion required to incorporate oxygen into the silicon crystal lattice in the formation of silicon dioxide can also contribute to the total stress.

We tested intentionally patterned cracks into the BOX layer for the purpose of improving yield in the release of two different types of silicon microcantilevers. The first device is an ultrasoft silicon cantilever specifically designed for magnetic resonance force microscopy (MRFM) [5]. The cantilever's shaft and paddle are 50 to 100 nm thick while

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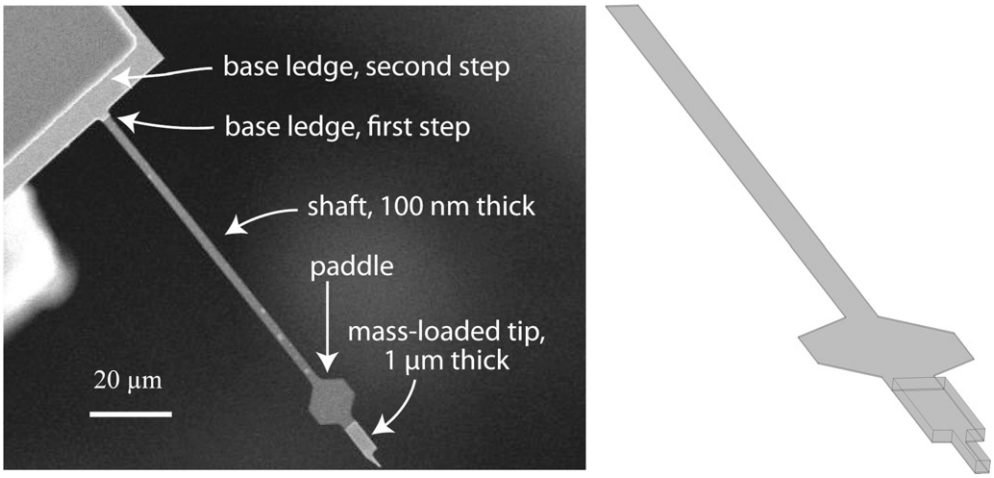

Figure 1. Scanning electron microscope image of an ultrasoft cantilever for magnetic resonance force microscopy (left) and the model drawing of the cantilever (right).

the tip is mass-loaded at 1 μm thickness (see figure 1). With stiffnesses on the order of 10^{-4} to 10^{-5} N m^{-1}, these single-crystal silicon cantilevers are extremely compliant. Their low stiffness is important for MRFM, which involves the measurement of very small forces, as low stiffness improves a cantilever's force sensitivity.

The compliance of these cantilevers, however, adds challenges to their manufacture. The BOX layer of SOI wafers is utilized as an etch stop during device release. As described earlier, the BOX membrane buckles and often cracks when the underlying silicon is removed. The cantilevers are formed from the device layer of the SOI wafer and generally survive substantial buckling of the BOX membrane. However, if a crack forms in the BOX layer and passes underneath a cantilever, the cantilever usually fractures. Cracking in the BOX layer has complicated the fabrication of similar MRFM cantilevers in prior manufacturing runs and resulted in considerable device losses during release.

The use of patterned cracks was also incorporated into the fabrication of a second type of device: piezoresistive silicon cantilevers for high-frequency force detection. These cantilevers are 300 nm thick with stiffnesses on the order of 10^{-2} to 10^{-4} N m^{-1}. Related cantilevers were previously fabricated with higher yield [6], but design and fabrication changes in the most recent version of these devices substantially reduced yield when they were fabricated without cracks patterned into the BOX layer.

In the fabrication of both types of silicon cantilevers presented here, we designed and lithographically patterned cracks into the BOX layer prior to device release to direct crack formation to non-critical areas of the oxide membrane. In addition to directing cracking away from the immediate vicinity of the cantilevers, the patterned cracks also allow for the in-plane expansion of the oxide membrane, much like expansion joints in a bridge.

Previous work has investigated cracking in tensile films using stiffeners [7–9]. Also, Kim *et al* employed break lines etched in tensile phosphosilicate glass to reduce cracking and improve their device survival [10]. In this work, we direct cracking in compressive silicon dioxide by lithographically patterning cracks into the layer prior to release. By influencing crack formation in the released oxide membrane, we seek to reduce cracking near or under delicate microdevices and thus improve yield.

2. Design

The purpose of this work is to evaluate the use of patterned cracks as an aid to device release in the manufacture of compliant microdevices with SOI wafers. Two different types of devices were used for testing this concept: ultrasoft silicon microcantilevers, designed for MRFM, and piezoresistive silicon microcantilevers for high-frequency force detection.

2.1. Ultrasoft cantilevers

Figure 1 shows both a scanning electron micrograph and a model drawing of a typical ultrasoft cantilever for MRFM. These single-crystal silicon cantilevers have shaft thicknesses of 50 to 100 nm, a mass-loaded region at the tip 1 μm thick, lengths of 85 to 200 μm, and stiffnesses of 5 to 150 μN m^{-1}. A paddle between the shaft and the mass-loaded tip increases the area available for optical reflection. A variety of shaft dimensions and tip shapes were included in this fabrication process for MRFM experiments. Also, a silicon ledge built up 2 to 3 μm tall at the base of the shaft clamps the cantilever. Lacking the ledge, the cantilever's length would be set by the imprecise backside etch through the handle wafer.

Two crack patterns were quantitatively evaluated following preliminary qualitative testing of several designs in the previous fabrication runs of MRFM cantilevers. Inspired by promising preliminary results [11], this work includes additional data and more detailed analysis of a much larger number of devices. The two crack pattern designs tested are shown in figure 2: (i) a 'moat' that encircles the cantilevers at the end of each die and (ii) a larger 'Y'-pattern. Each die has three MRFM cantilevers, and was fabricated with either a moat crack pattern, the Y-pattern, or no crack pattern. Due to

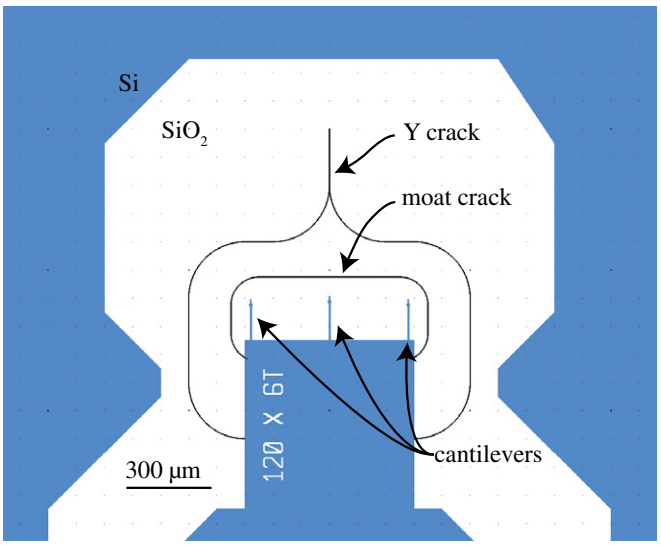

Figure 2. Ultrasoft cantilever mask image of crack patterns (black) with the topside silicon pattern (blue) against the BOX layer (white). Three cantilevers protrude from the broad snout of the die. While both crack patterns are shown here, only one crack pattern per die was used. A smaller moat pattern was used for the die with shorter cantilevers. Adapted from [11].

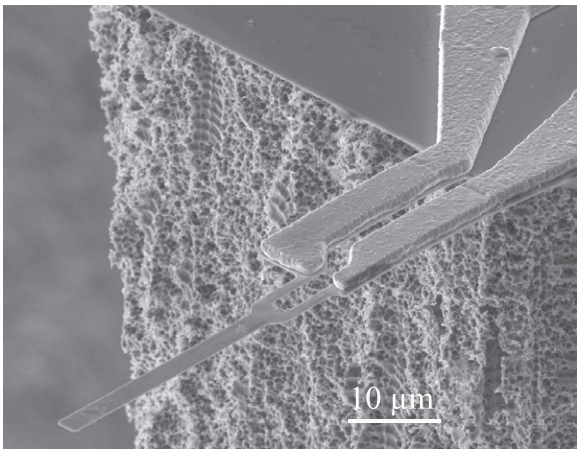

Figure 3. Scanning electron microscope image of the piezoresistive cantilever for high-frequency biomolecular and cellular force sensing.

the range in cantilever lengths in this fabrication run, a smaller moat pattern was used for shorter cantilever designs. Each wafer of ultrasoft cantilevers included a representative subset of the die processed without patterned cracks to enable a well-controlled evaluation of the effectiveness of the crack patterns.

2.2. Piezoresistive cantilevers

Figure 3 shows a scanning electron micrograph of a piezoresistive silicon cantilever for high-frequency biomolecular and cellular force sensing. These single-crystal silicon cantilevers are 300 nm thick, 1 to 2 μm wide, and 30 to 200 μm long with estimated stiffnesses from 300 μN m^{-1} to 80 mN m^{-1}. In contrast to prior work [6], these cantilevers

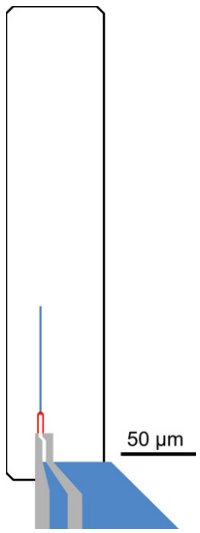

Figure 4. Piezoresistive cantilever mask image showing the crack pattern (black), BOX layer (white), metal layer (gray), and topside silicon pattern without diffusion doping (blue) and with diffusion doping for the piezoresistive sensors at the base of the cantilever (red).

have an asymmetric base that protrudes from the corner of the die and the base includes a topside stiffener made from 1 μm thick aluminum. As with the ultrasoft cantilevers, this stiffener sets the clamping condition for the cantilever beam, and allows for precise control over the effective cantilever length. The positioning of the cantilever near the corner of the die facilitates physical access to the force sensor during use. The combined effects of these design modifications increase the susceptibility of the cantilever to fracture from cracks in the BOX layer during release processing.

The crack pattern used on the piezoresistive cantilevers is shown in figure 4. The use of this moat-type crack pattern was quantitatively evaluated by recording the cantilever yield in two separate fabrication runs. No patterned cracks were used in the first fabrication run, while patterned cracks were used on all dies in the second fabrication run. This experimental design provides less control of confounding variables, such as wafer-to-wafer variations in process conditions or fabrication variations that affect an entire lot, than the well-controlled test of patterned cracks implemented in ultrasoft cantilever fabrication. However, the experiment conducted with piezoresistive cantilever fabrication provides additional data on the utility of patterned cracks in a different fabrication process, and in the production of a different type of device with a stiffer range of compliance values than the ultrasoft cantilevers.

3. Fabrication

3.1. Ultrasoft cantilevers

The fabrication process for ultrasoft cantilevers is shown in figure 5 and was adapted from prior work on cantilevers for MRFM [12]. SOI wafers with a silicon device layer thickness of 340 or 450 nm and a BOX layer thickness of 1000 nm were

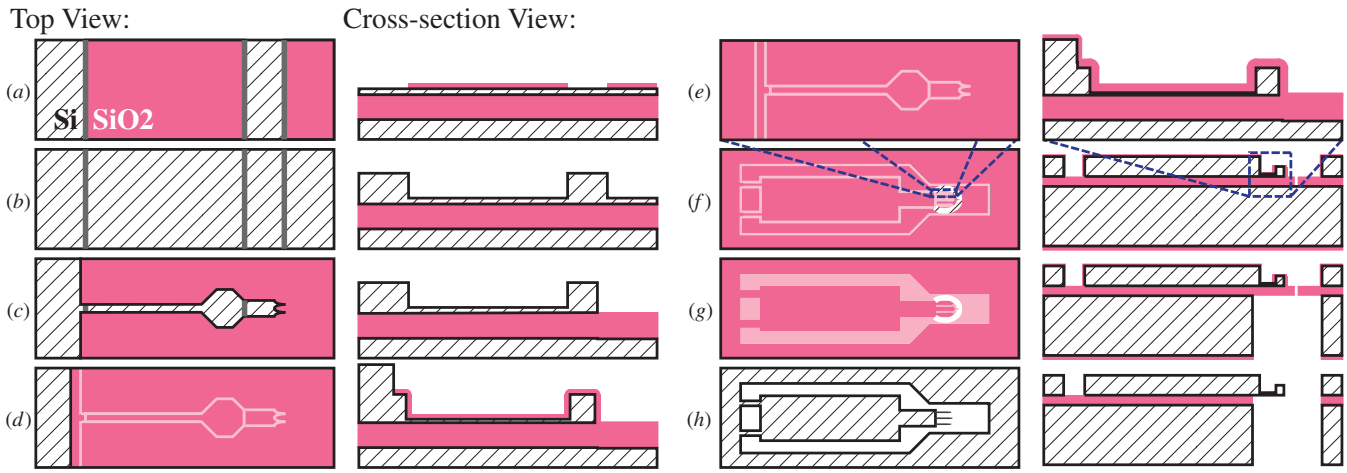

Figure 5. Fabrication process for ultrasoft cantilevers. (*a*) An oxide hard mask is thermally-grown and patterned on a silicon-on-insulator wafer. (*b*) A 1 μm layer of epitaxial silicon is selectively grown on the exposed silicon of the device layer to form the mass at the cantilever's tip and the first step of the base ledge; the oxide hard mask is subsequently removed. (*c*) The cantilever is patterned with a silicon plasma etch. (*d*) A second layer of epitaxial silicon is selectively grown to increase the ledge at the base of the cantilever using another thermally-grown oxide hard mask. (*e*) A third thermal oxidation tunes the cantilevers' shaft thickness to 100 nm. (*f*) Cracks are patterned and etched into the BOX layer. (*g*) A deep reactive ion etch from the backside of the wafer removes the silicon handle wafer underneath the cantilever. Photoresist (not shown) is used to protect the front side of the wafer and is subsequently stripped. (*h*) A hydrofluoric acid vapor etch removes the BOX and front side oxide, releasing the cantilevers.

used as the starting material. A long, high temperature anneal in nitrogen at 1100 °C was used to reduce stress in the BOX–silicon interface prior to further processing. Two selectively-grown epitaxial silicon layers were deposited to build up the mass at the cantilevers' tips and the ledges at the cantilevers' bases. Oxide hard masks were used during the epitaxial silicon deposition. A silicon plasma etch defined the cantilevers from the device layer. A series of thermal oxidations formed the oxide hard masks and thinned the device layer to its final thickness.

Prior to release, crack patterns were etched 80–100% through the BOX layer using a reactive ion plasma etch for oxide. While this etch was timed for significant overetch so as to fully etch through the BOX layer, some polymer built-up or redeposition of photoresist in the exposed features retarded the etch and sometimes resulted in shallower crack pattern trenches. We estimate from in-process measurements of the etch depth that cracks etched approximately 80% or more through the BOX layer were sufficient to later initiate cracking along the crack pattern, but shallower cracks were ineffective. Wafers with shallower crack pattern etches were excluded from later analysis; these wafers were easily identifiable in that no cracks formed along the crack pattern when the oxide membrane was released.

Figure 6(*a*) shows an optical microscope image of a die with no crack pattern prior to release, while figure 6(*b*) shows a die with the moat pattern etched into the BOX layer prior to release. Figures 6(*c*) and (*d*) correspond to figures 6(*a*) and (*b*), respectively, by showing a similar die after the BOX membrane was released using a deep reactive ion etch (DRIE) through the wafer from the backside. The buckling and cracking of the BOX layer is evident in the images, and in figure 6(*d*) the interior of the moat pattern forms a distinct membrane from the rest of the BOX layer.

In release processing, the front side of the wafer was coated with photoresist for protection during DRIE; this photoresist protection layer also improved device yield relative to wafers lacking the protection layer. The photoresist layer was also useful in protecting the topside devices during the final portions of the DRIE, when cracks in the BOX layer allow plasma gases access to the front side of the wafer. Of note is that process gases do access the topside of the wafer during the final minutes of the DRIE through either patterned cracks or spontaneous cracks in the BOX layer. The photoresist was later stripped in an oxygen plasma asher. The wafers were carefully cleaned in hot sulfuric acid and hydrogen peroxide and rinsed in water; special effort was made to gently handle the wafers during these steps and to minimize the fluid forces on the delicate BOX membranes. The final device release was accomplished with a hydrofluoric acid vapor etch that removed the BOX membrane and front side oxide. The wafers were visually inspected during release processing after every critical step and each cantilever was evaluated and scored for survival.

3.2. Piezoresistive cantilevers

The piezoresistive cantilevers were fabricated in a six-mask process adapted from prior work [6]. SOI wafers were used with a 340 nm thick device layer and a 400 nm thick BOX layer. First, the device layer was oxidized to form a diffusion mask and to thin the device layer to 300 nm. Next, residual stress and stress gradients were reduced with the same high temperature anneal as applied to the ultrasoft cantilevers. Windows were opened in the oxide mask with hydrofluoric acid and the wafer was phosphorus doped using $POCl_3$ predeposition at 775–850 °C to form the piezoresistors and contacts. The

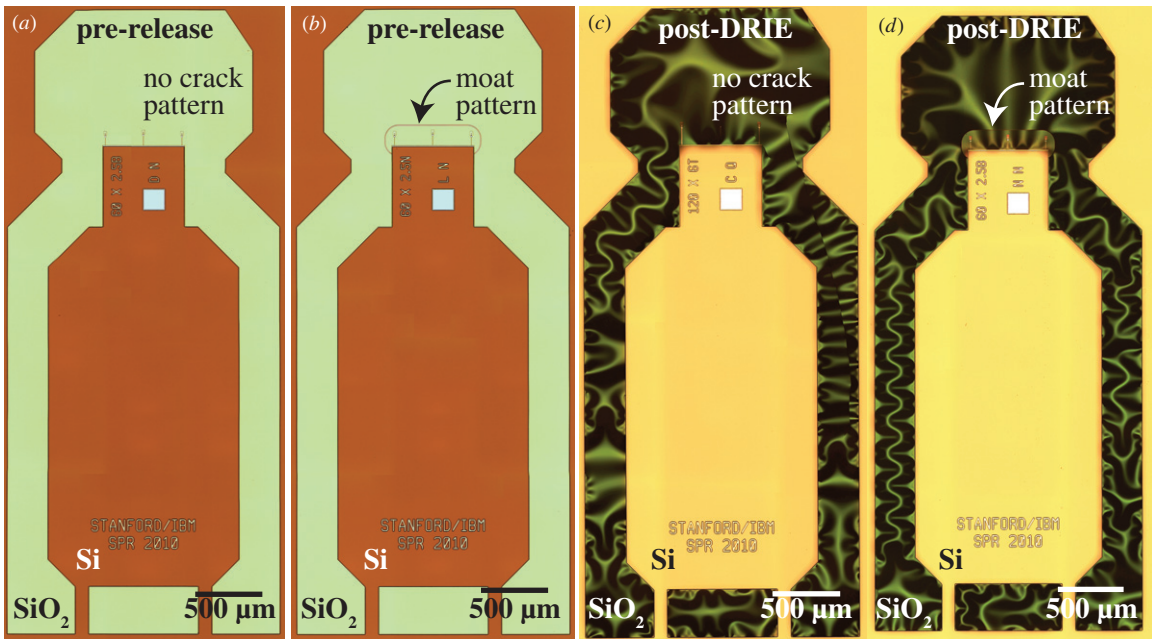

Figure 6. Optical microscope images of the ultrasoft cantilever die before (*a*,*b*) and after (*c*,*d*) the removal of the silicon handle wafer beneath the BOX layer during release processing. In (*a*,*c*), no crack pattern was used while in (*b*,*d*), the moat pattern was etched into the BOX layer. The BOX layer shows evidence of ripples and cracks when released in (*c*, *d*). Also, in (*d*), the moat crack pattern defines a separate membrane formed from the BOX layer. See figure 7 for more detail.

diffusion mask was stripped and a silicon plasma etch defined the cantilevers and piezoresistors in the device layer.

A 200–400 nm thick low-pressure chemical vapor deposition (LPCVD) silicon dioxide dielectric layer was deposited at 400 °C and via windows were opened using hydrofluoric acid. Titanium and aluminum layers, 40 and 1000 nm thick, respectively, were sequentially deposited by sputtering. Titanium was used to reduce the contact barrier height and to serve as a diffusion barrier to prevent aluminum spiking. The metal layers were patterned by reactive ion etching, and the wafer was encapsulated in a 300 nm thick LPCVD silicon dioxide coating to protect the aluminum and silicon during the release process. Cracks were etched completely through the LPCVD oxide and BOX layers by reactive ion etching and the backside of the wafer was lithographically patterned to define the DRIE release step.

Before the backside etch, the wafer was attached to a carrier wafer using Crystalbond 555 (SPI Supplies, West Chester, PA). DRIE was performed remotely (University of Michigan, Ann Arbor, MI) and the carrier wafer stabilized the device wafers for shipping. No front side photoresist was used because it reacted with the Crystalbond. After the DRIE process, residual C_4F_8 polymer on the BOX was removed in a reactive ion etcher using an O_2 plasma with 10% SF_6 to make the fluoropolymer volatile. Finally, the wafer was carefully detached from the carrier in 70 °C deionized water and the cantilevers were released using a hydrofluoric acid vapor etch. After fabrication, each wafer was visually inspected and its cantilevers were scored for survival.

Table 1. Percent cantilever survival by the crack pattern used for three processed wafers of ultrasoft cantilevers. The total number of devices tested is in parentheses. Devices with and without patterned cracks were fabricated on the same wafer.

	No crack pattern	Moat pattern	Y-pattern	Overall
Wafer 1	45% (210)	61% (423)	35% (213)	50% (846)
Wafer 2	25% (210)	74% (423)	34% (213)	52% (846)
Wafer 3	66% (210)	81% (636)	–	77% (846)
Overall	46% (630)	73% (1482)	35% (426)	60% (2538)

4. Results

4.1. Ultrasoft cantilevers

The final survival data for the ultrasoft cantilevers are listed in table 1. The percent yield is shown for three wafers, including a breakdown based on the crack pattern used. The die processed with no crack pattern had an average survival of 46%, while the moat pattern improved survival to 73%. The Y-crack pattern had an overall survival of 35%.

Wafer-to-wafer variations play a role in interpreting these yield statistics. Due to poor initial results with the Y-pattern, its use was discontinued in the third wafer in favor of the moat crack pattern. However, the third wafer also had the highest yield values of any wafer for all of the designs. The improved performance of the third wafer is especially apparent when comparing the yield of the die processed without any patterned cracks between the three wafers. Wafers 1 and 2 had an average yield of 35% when no crack pattern was used, while wafer 3 had an average yield of 66% for similar devices. The three wafers were fabricated in the same run,

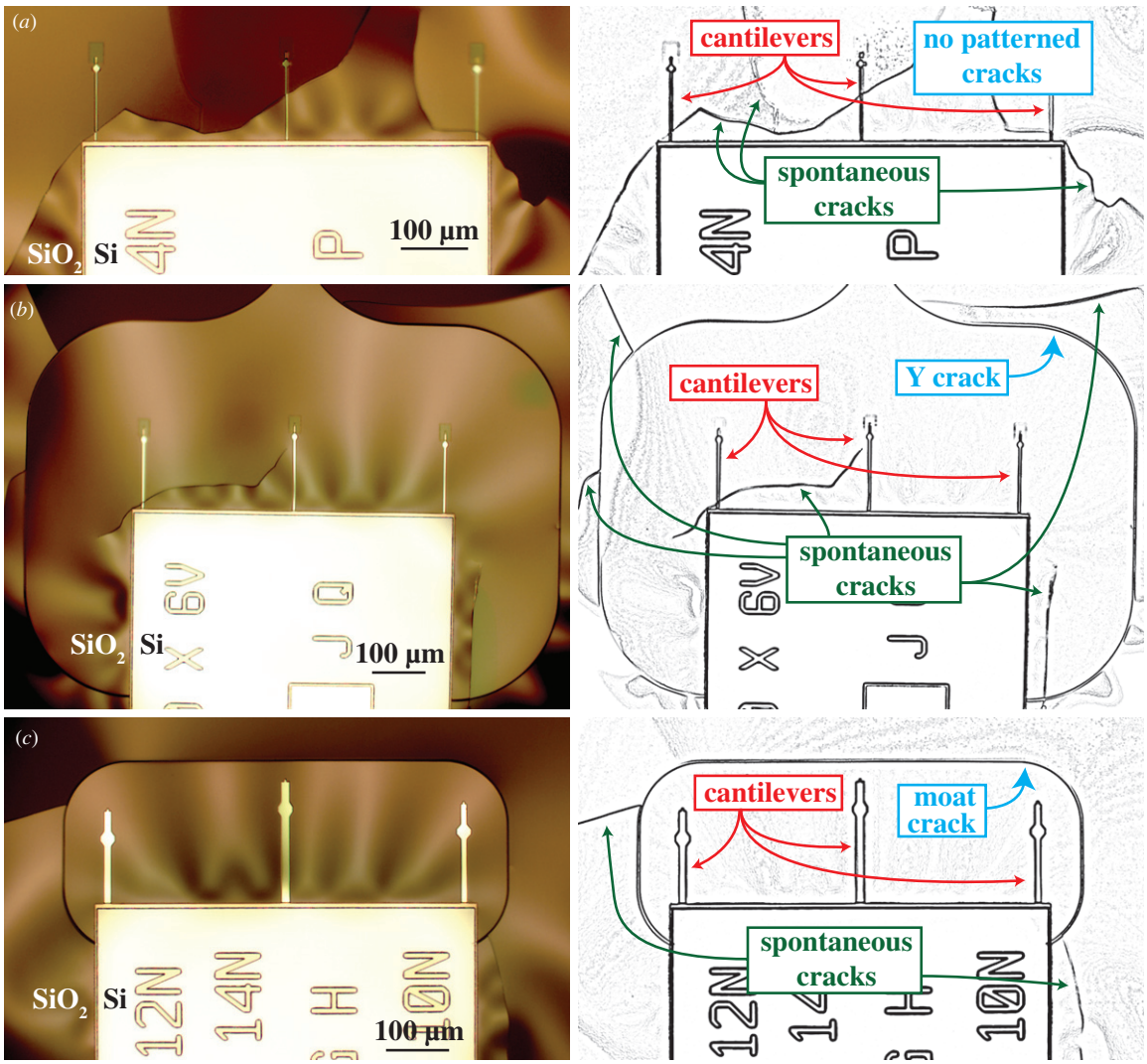

Figure 7. Optical microscope images of buckling and cracking in the BOX membrane during the release processing of ultrasoft cantilevers. Original images are shown on the left. The same images are shown on the right after edge-finding image processing and with features labeled. (*a*) No crack pattern was used and all three cantilevers are fractured by spontaneous cracks in the BOX membrane. (*b*) The Y-crack pattern was used, and several spontaneous cracks outside the pattern terminate at the patterned crack. One spontaneous crack in the lower right crosses the pattern but does not reach the cantilevers. However, the pattern is large and the left cantilever is fractured by a spontaneous crack that formed entirely within the pattern. (*c*) The moat crack pattern was used, and all three cantilevers survive. Several spontaneous cracks terminate at the patterned crack and do not cross it.

though release processing proceeded serially rather than in parallel. However, no differences in process or handling were identified that might account for the yield variation between these wafers. To account for the variability in yield between wafers, a Cochran–Mantel–Haenszel (CMH) test with continuity correction was used to analyze the results. Using data from all three wafers, the higher yield with the moat crack pattern is significantly different from the lower yield with no crack pattern $\left(\chi^2_{\mathrm{CMF}} = 132,\ 1 \text{ degree of freedom},\ p = 1.2 \times 10^{-30}\right)$. In contrast, the Y-crack pattern yield is not significantly different from the no crack pattern yield according to a CMH test on results from the first two wafers $\left(\chi^2_{\mathrm{CMF}} = 0.023,\ 1 \text{ degree of freedom},\ p = 0.88\right)$.

These results can be qualitatively understood from the optical microscope images of the freed BOX membrane and cantilevers during release processing (figure 7). These images were taken after removal of the handle wafer with DRIE but prior to final cantilever release with oxide etching. The original images are on the left, and the versions shown on the right were subject to edge-finding image processing and labeling. Without patterned cracks, spontaneous membrane cracks frequently ran beneath the cantilevers and fractured them (figure 7(*a*)). The outer cantilevers were particularly stricken by cracks that formed near the corners of the die, which acted as stress concentrators. An example of corner cracks threatening but not yet fracturing outer cantilevers is shown in figure 8. The patterned cracks successfully terminated many spontaneous cracks and prevented them from propagating toward the cantilevers. However, the Y-pattern was too large and spontaneous cracks often formed inside the pattern (figure 7(*b*)). The moat pattern was far more effective in protecting the cantilevers. Figure 7(*c*) shows the moat pattern terminating two spontaneous cracks and keeping

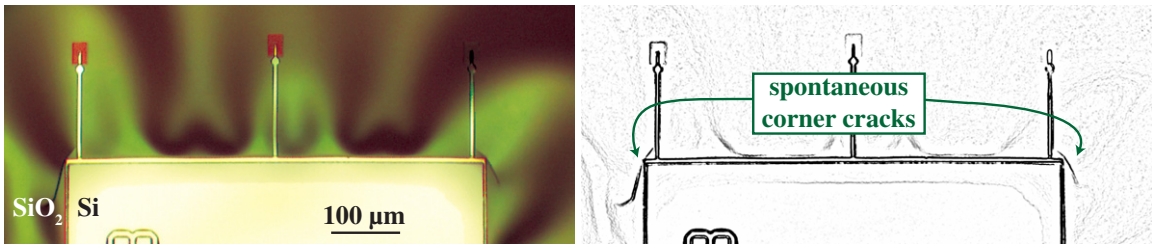

Figure 8. Optical microscope image of spontaneous cracks that formed in the oxide membrane near the corners of the silicon ledge during the release processing of ultrasoft cantilevers (left). For clarity, the same image is shown with edge-finding image processing (right).

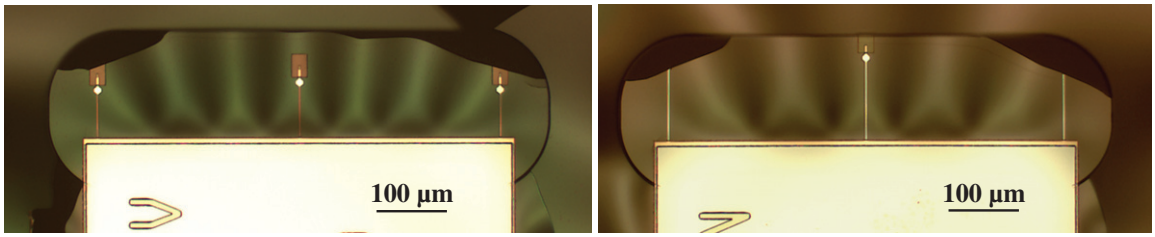

Figure 9. Optical microscope image of cracking on the unsupported corners and edges of the oxide membrane formed inside the moat pattern during the release processing of ultrasoft cantilevers. The moat patterns used for each die were of the same size, but the cantilevers on the left are shorter than those on the right by design. The shorter cantilevers are sufficiently inset from the crack pattern to survive in spite of fractures clipping the corners of the BOX membrane formed inside the moat pattern. Longer outer cantilevers on the right are sheared off by similar fractures clipping the unsupported corners of the BOX membrane.

them from propagating toward the cantilevers; also fewer cracks formed inside the moat pattern relative to the Y-crack pattern.

While the crack patterns did protect the microdevices from the propagation of spontaneous cracks, they also introduced another risk in the vicinity of the cantilevers. The BOX membrane formed inside both the moat and Y-patterns was free-standing on three sides, and sometimes fractured at its unsupported corners and edges far from the die, as shown in figure 9. In the right image of figure 9, the tips of the outer cantilevers were sheared off by cracks clipping the upper corners of the oxide membrane inside the moat pattern. In the left image, the moat pattern used is of the same size as on the right and similar cracks clipping the membrane corners are evident. However the cantilevers on the left die survive as they are shorter than those on the right by design, and thus there is a larger standoff distance between the cantilever and the crack pattern.

The importance of the standoff distance between cantilevers and the corners and edges of the oxide membrane formed by the crack pattern was recognized after an anomalous finding on the first wafer processed. The survival of cantilevers of a particular length (130 ± 6 μm) was lowered by the use of the moat crack pattern. These medium-length cantilevers were paired with the smaller moat pattern of the two available on the mask set for a cantilever tip-patterned crack standoff distance of approximately 20 μm. In contrast, on the same wafer, the small moat pattern improved the survival of shorter cantilevers and the larger moat pattern improved the survival of longer cantilevers. On subsequent wafers, these medium-length cantilevers were paired with the larger moat pattern for a distance of almost 100 μm between the end of the cantilever and the edge of the crack pattern. This combination showed an increased survival of the medium-length cantilevers when compared to those processed with no patterned cracks (table 2). This finding is also consistent with results from the preliminary testing of earlier crack pattern designs. Those qualitative studies suggested that crack patterns very closely encircling each cantilever were, at best, not beneficial and possibly detrimental to cantilever survival.

Table 2. Percent cantilever survival by moat pattern used for ultrasoft cantilevers of length 124 to 136 μm. The survival of a similar die on the same wafer with no crack pattern used is shown for comparison. The total number of devices tested is in parentheses.

Moat pattern	Tip-moat spacing	Moat survival	No crack survival
Small	~20 μm	40% (93)	57% (69)
Large	~95 μm	77% (255)	40% (138)

4.2. Piezoresistive cantilevers

Table 3 shows the survival of piezoresistive cantilevers fabricated with and without patterned cracks. Six wafers were processed in the first run without any patterned cracks, and these wafers had an average yield of 35%. Four wafers were processed in a subsequent run that utilized patterned cracks, and these wafers had an average yield of 69%, nearly double the previous result.

Similar to the results for the ultrasoft cantilevers, the optical microscope images of the BOX membranes formed

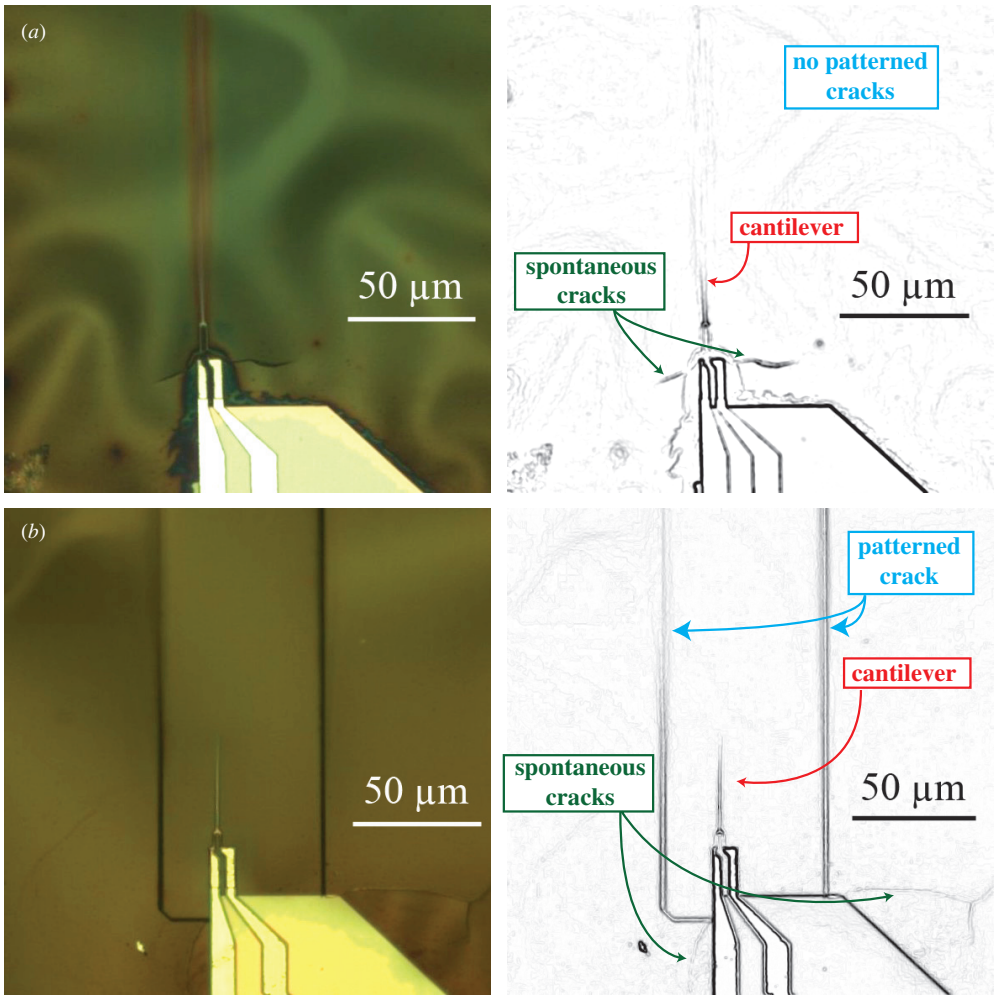

Figure 10. Optical microscope images of the BOX membrane and piezoresistive cantilevers during release processing. Original images are shown on the left, and the same images are shown on the right after edge-finding image processing and with features labeled. (*a*) Without a crack pattern, the BOX consistently cracked at the end of the aluminum stiffener, separating the cantilever from its base. (*b*) A pattern crack surrounds the device and spontaneous cracks are visible outside but not inside the patterned crack.

Table 3. Percent piezoresistive cantilever survival based on the use of the crack pattern. Each wafer contained 99 dies with two cantilevers each (198 total). Wafers with and without the patterned cracks were fabricated in separate runs.

	No crack pattern Fabrication Run 1	Moat pattern Fabrication Run 2
Wafer 1	21%	73%
Wafer 2	47%	63%
Wafer 3	38%	90%
Wafer 4	50%	51%
Wafer 5	16%	–
Wafer 6	40%	–
Overall	35%	69%

during the release of the piezoresistive cantilevers help illustrate the protective action of the patterned cracks. In figure 10(*a*) with no patterned crack, spontaneous cracks are visible near the base of the cantilever. Without patterned cracks, the silicon cantilever reliably broke at the end of the aluminum stiffener due to spontaneous cracking in this location. In figure 10(*b*) with the crack pattern etched into the BOX layer, spontaneous cracks exist outside the patterned crack but not inside it.

The yield-improving crack pattern used with the piezoresistive cantilevers had a minimum standoff distance of 20 μm from the cantilever to the crack pattern. This is in contrast to the yield-lowering combination of the small moat crack pattern with medium-length ultrasoft cantilevers and a 20 μm standoff distance as discussed in 4.1. However, for the piezoresistive cantilever, the minimum standoff distance occurs between the side of the cantilever and the crack pattern's left edge as shown in figure 4. With the ultrasoft cantilever, the minimum standoff distance occurs between the cantilever's tip and the far corner of the crack pattern. The distance between the piezoresistive cantilever's tip and the far corner of the crack pattern varied with cantilever length from 100 to 270 μm. The far corners of the BOX membrane formed inside the various crack patterns are unsupported and subject to fracture as in figure 8. It may be that the 20 μm distance between the cantilever and the crack pattern is not a problem in general, but only when such a distance puts the microdevice

in the vicinity of fragile edges or corners formed in the BOX membrane during release.

Another variable to consider is that the wafers used in the piezoresistive cantilever fabrication had a BOX layer thickness of 400 nm, while the ultrasoft cantilevers were fabricated from wafers with 1000 nm thick BOX layers. The thickness of the BOX layer affects its compliance and the buckling pattern adopted by the oxide membrane when released. In addition, the BOX layer thickness can affect the fracture incidence of released BOX membranes. Two SOI wafers with a 1000 nm BOX layer were included in the first fabrication run of piezoresistive cantilevers without patterned cracks. These two wafers, not included in table 3, had an average yield of 15% rather than 35% from the six wafers with a 400 nm BOX layer. Thus the optimum crack pattern design, including the optimum standoff distance, may vary with the BOX thickness, the geometry of a given device, and the clamping conditions imposed on the BOX membrane by both the remaining silicon handle wafer after device release and any topside stiffeners.

The experiment evaluating the effectiveness of BOX-layer crack patterning in piezoresistive cantilever fabrication was not as well controlled as in the experiment conducted with ultrasoft cantilevers. Wafer-to-wafer variation, iterative improvements in wafer processing and handling, and the several months that elapsed between processing the two piezoresistive cantilever runs might also affect the results. However, the magnitude of the improvement between the two runs provides additional support for the utility of patterned cracks in microdevice release. The range of yields observed without patterned cracks (16–50%) and with patterned cracks (51–90%) do not overlap.

5. Conclusions

Cracks patterned directly into the buried oxide layer were found to significantly improve yield in the release of delicate microdevices. In the fabrication of ultrasoft cantilevers, the use of a moat crack pattern improved the overall cantilever survival rate from 46% to 73%, an improvement of more than 60%. A larger Y-crack pattern was also tested and found to be ineffective as it allowed cracks to form and propagate inside the pattern. Additionally, the unsupported edges and corners of the BOX membrane formed inside both types of crack patterns were susceptible to fracture, and this decreased the survival of devices that extended too close to the patterned crack. Patterned cracks in the BOX layer were also found to improve device yield in a second microfabrication process. The yield of piezoresistive cantilevers improved by more than 95% from an average yield of 35% without crack patterns to 69% with a moat-type crack pattern. These results are important for the fabrication and safe release of compliant structures using SOI wafers.

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